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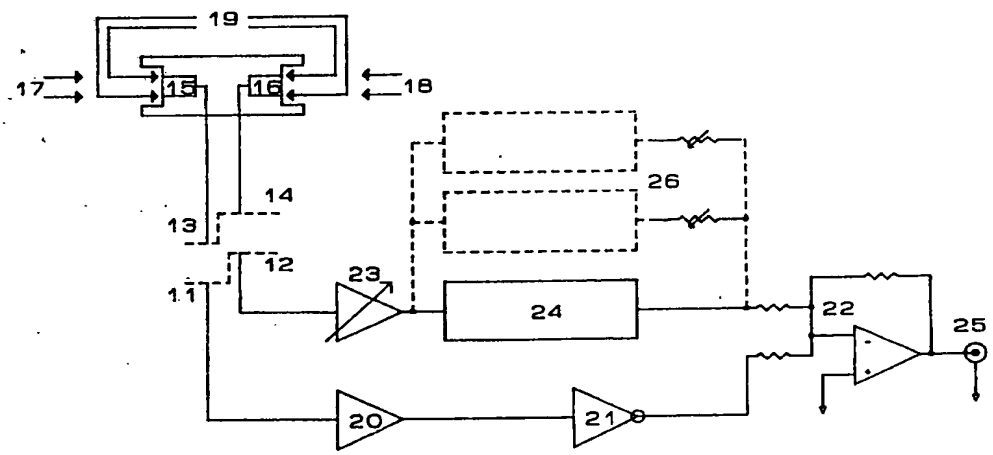

(57) Abstract

This invention relates to a circuit for processing output signals from at least two microphones spaced relative to a sound source. Circuit (10) has inputs (11, 12) which are connected to the respective outputs (13, 14) of microphones (15, 16). The microphone (15) is directed to a sound source (17) whilst the microphone (16) is directed away from that sound source. A sound path (19) is defined between the microphones (15, 16). The inputs (13, 14) are connected to a summing junction (22) via respective amplifiers (20, 23) and in one channel the signal is inverted and in the other channel the signal is delayed. By suitable adjustment of gain and delay, the circuit can be arranged to either cancel noise generated from a sound source other than (17) and/or to adjust the directionality of the microphone system.

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A Circuit for use with Microphones

This invention relates to a circuit for processing output signals from at least two microphones spaced relative to a sound source.

It has been proposed for sometime to form a directional microphone by using a single diaphragm with a cavity on each side. Each cavity is connected to a respective input and the input which is furthest away from the sound source of interest is provided with an acoustic delay in the form of baffles and the like creating a longer sound path. If the spacing between the inputs and the delay created within the rear input are each equivalent to $\lambda/4$ then sounds received from the direction of the intended source are effectively added at the diaphragm, but sounds reaching the rear input first are cancelled at the diaphragm. This arrangement has several disadvantages: first it is very difficult to adjust the acoustic delay, secondly it takes no account of the loss in sensitivity between the rear and front inputs and hence cancellation is incomplete and thirdly it is extremely frequency dependent.

From one aspect the invention provides a circuit for processing output signals from at least two microphones spaced relative to a sound source and producing respective output signals, comprising an input for each microphone, means for time delaying the output signals of all the microphones bar one relative to the output signal of said one in accordance with the intended relative spacing between

each microphones and said one microphone; means for inverting the output of the one microphone or the outputs of the other microphones or microphone; means for attenuating or amplifying one or more of the output signals so as to select the relative amplitudes of the output signals derived from sources other than the sound source and means for summing the processed output signals to provide a final output signal.

The delay means may delay signals after they have passed through the inverting means and/or the amplifying and attenuating means and indeed the order of processing is not important and the inversion and gain adjustment can be carried out on either set of signals. The time delay means are preferably pure time delay means so that they do not introduce phase shifting and thus, at least over the audio range, are substantially frequency independent. For example, they may be constituted by a linear all pass filter, a digital delay line or surface wave device. Similarly it will be understood that the invention covers circuits in which the one output signal is phase shifted by 360° or a multiple thereof.

It is particularly preferred that the gain of the amplifying or attenuating mean is adjustable and can be used to either equate the output signals for full cancellation or to adjust the degree of directionality and that the or/each delay means is adjustable.

The invention also includes a microphone system comprising a microphone and a circuit as defined above, the

output of the microphone being connected to an input of the circuit.

Preferably there is a plurality of microphones each connected to a respective input of the circuit and the one microphone is that which is intended to be nearest the desired sound source. The microphones may be physically connected, in which case they may be acoustically decoupled, and in any event they may be arranged in a line. The microphones at the ends of the line may be directed in opposite directions, but other orientations can be used with suitable adjustment of the delay means.

In one convenient embodiment there are two microphones mounted on a single head in opposed relationship.

Although the invention has been defined above it is to be understood that it includes any inventive combination of the features set out above.

A invention may be performed in various ways and will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram of an embodiment of a circuit for processing output signals from two microphones; and

Figure 2 shows a diagram of a typical directionality response.

Referring to Figure 1 a circuit is generally indicated at 10 and has inputs 11,12 to which are connected the respective outputs 13,14 of omni-directional microphones 15,16.

The microphones 15,16 are mounted in a housing so that they are held at a fixed spacing and are oppositely directed. In use it is intended that the microphone 15 should be directed towards a sound source 17 whilst the microphone 16 is directed away from that sound source. A sound path 19 is defined between the microphones 15,16 around the side of the housing. It will be understood that sound will arrive at one or other of the microphones first and the delay between that sound being received at the other microphone is a function of the length of the sound path 19. The length of the sound path 19 is preferably shorter than one wavelength of the maximum frequency to be cancelled and may desirably be less than one half of that wavelength.

Turning to the circuit 10, the input 11, which is related to the main sound microphone 15, is connected via a buffer amplifier 20 and a signal inverter 21 to a summing junction 22. The input 14 is connected to receive the output of the rearward facing microphone 16 and again has a buffer amplifier 23, but this time with an adjustable gain. The output of the amplifier 23 is fed to a main time delay 24 which is selected to produce a pure time delay equal to that created by the sound path 19. The output of the delay 24 is fed to the summing junction 22 where it is combined with the output of the invertor 21 to produce a final output signal at 25.

If the delay created by the sound path 19 and the main time delay 24 are approximately equal for the received sound from the main sound source 17, then the inputs to the

summing junction 22 will substantially add due to their phase shifting. If however a sound comes from a source whereby it will be first received by the microphone 16 e.g.from 18) then each signal will be delayed by the same amount and the signals derived from that sound will be cancelled out. The result is thus that the background noise can be to a great extent removed from the signal available at a 25.

Because the gain of amplifier 23 is adjustable it is possible to compensate for the difference in signal strength derived from a sound from a particular location which arises from the microphones 15,16 because one is further from the source than the other. This means that the cancellation of the undesired signals, i.e. those first received by microphone 16, can be particularly accurate, with the result that the microphone creates very little acoustic feedback. The forward feedback characteristic (i.e. with the microphone 15 directed towards a loudspeaker receiving a signal from 25) can be particularly improved if the frequency of the signal at output 25 is arranged to have a flat frequency response or is subsequently processed to produce such a response.

The performance of the circuit 10 can be further improved by the introduction of parallel secondary delay paths indicated at 26. In particular these can be used to compensate for sounds which are located to the side of the microphones 15,16.

An even better performance can be achieved by increasing the number of microphones and preferably the microphones are arranged in a line. They may all be directed at right angles to the direction of sound from source 17 or only the intermediate ones may be so directed. In this arrangement each microphone will have a gain and delay channel connected respectively into the summing junction 22.

The effect of the overall system, as shown in Figure 1, is to provide a highly directional microphone, as shown in Figure 2, with an anti-noise performance and background noise and feedback by up to 30 dB with a single main delay. The addition of secondary delays can improve this noise and feedback cancellation still further. Alternatively, the circuit 10 can be used to adjust the directionality of the microphone on an infinitely variable basis.

It is envisaged that one commercial arrangement of the invention would be a microphone having the circuit 10 formed in its chip, with the microphone connected to one input of the circuit and the other input or inputs being arranged for connection to respective other microphones. Preferably the microphones would plug into each other so that arrays of different lengths could be built up.

It should be understood that the microphones 15,16 need not be omni-directional, particularly in multi-microphone arrays.

CLAIMS

1. A circuit for processing output signals from at least two microphones spaced relative to a sound source and producing respective output signals, comprising an input for each microphone, means for time delaying the output signals of all the microphones bar one relative to the output signal of said one in accordance with the intended relative spacing between each microphones and said one microphone; means for inverting the output of the one microphone or the outputs of the other microphones or microphone; means for attenuating or amplifying one or more of the output signals so as to select the relative amplitudes of the output signals derived from sources other than the sound source and means for summing the processed output signals to provide a final output signal.

2. A circuit as claimed in Claim 1, wherein the delay means delays signals after they have passed through the inverting means and/or the amplifying and attenuating means.

3. A circuit as claimed in Claim 1 or Claim 2, wherein the inversion and/or gain adjustment is carried out on one set or the other set of signals.

4. A circuit as claimed in any one of the preceding Claims, wherein the time delay means are pure time delay means.

5. A circuit as claimed in Claim 4, wherein the time delay means are constituted by a linear all pass filter, a digital delay means or surface wave device.

6. A circuit as claimed in any one of the preceding

Claims, wherein the gain of the amplifying or attenuating means is adjustable whereby the output signals can be equated for full cancellation or the degree of directionality can be adjusted.

7. A circuit as claimed in any one of the preceding Claims, whereby the delay means is adjustable.

8. A circuit as hereinbefore described with reference to the accompanying drawings.

9. A microphone system comprising a microphone and circuit as claimed in any one of the preceding Claims, wherein the output of the microphone is connected to an input of the circuit.

10. A system as claimed in Claim 8, wherein there is a plurality of microphones each connected to a respective input of the circuit and wherein the one microphone is that which is intended to be nearest the desired sound source.

11. A circuit as claimed in Claim 10, wherein the microphones are physically connected but at least substantially acoustically decoupled.

12. A system as claimed in Claim 10 or Claim 11, wherein the microphones are arranged in line.

13. A system as claimed in Claim 12, wherein the microphones at the ends of the lines are directed in opposite directions.

14. A system as claimed in Claim 13, wherein there are two microphones mounted on the single head in opposed relationship.

15. A microphone system substantially as hereinbefore described.

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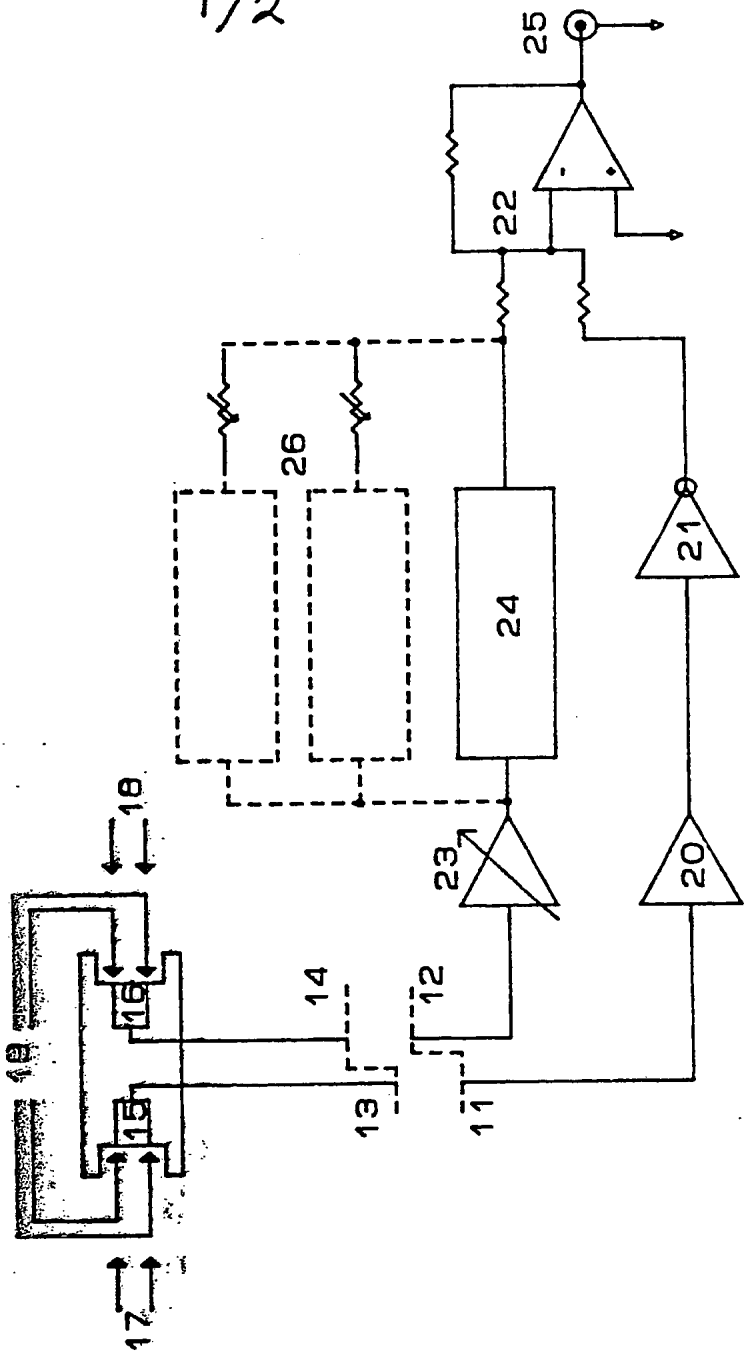

FIGURE 1

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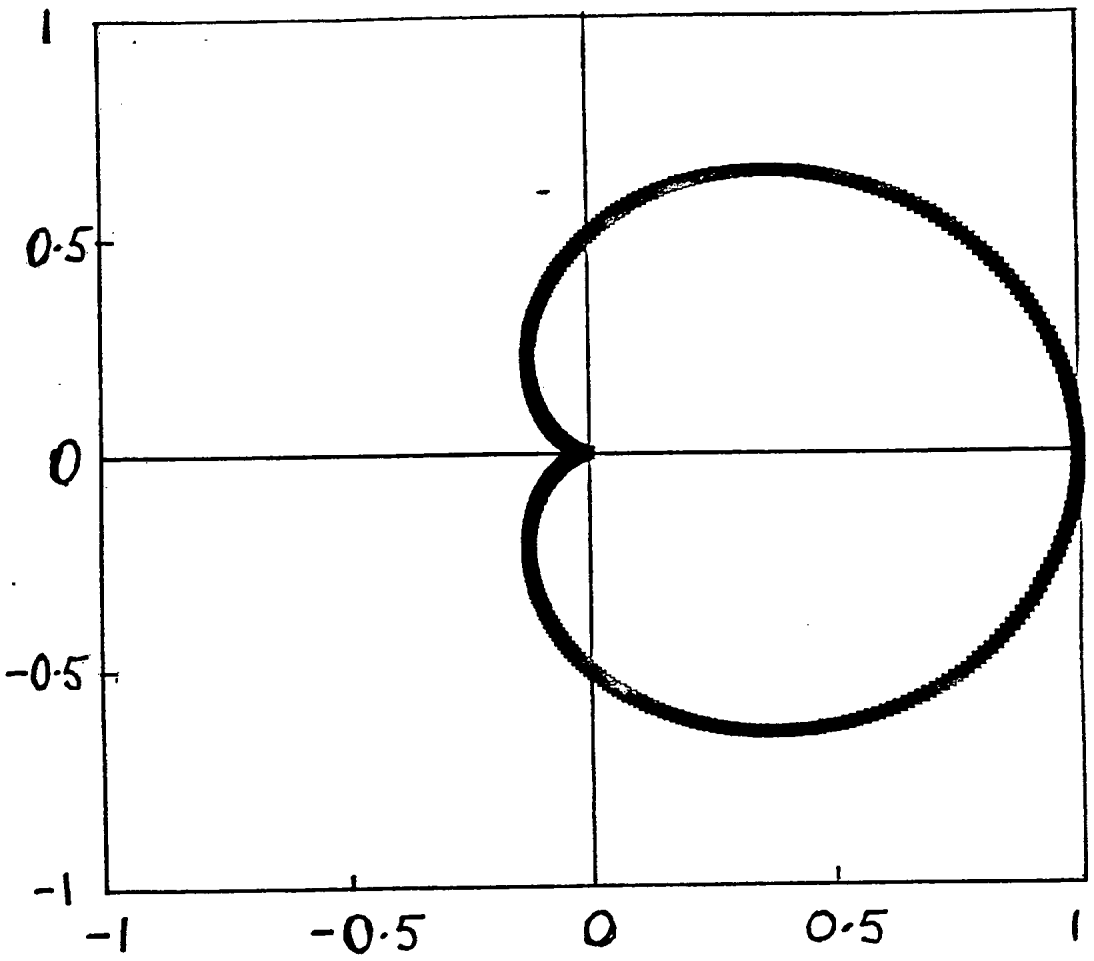

FIGURE 2

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 92/02127

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[5]: H 04 R 1/40

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[5]	H 04 R,H 04 M

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	DE, A1, 3 325 815 (SHURE) 05 April 1984 (05.04.84), see abstract; page 7, line 1 - page 10, line 6; fig. 2; claims 1-4. --	1
A	DE, A1, 3 033 985 (VICTOR COMP.) 09 April 1981 (09.04.81), see page 4, line 1 - page 8, last line; fig. 1; claim 1. --	1
A	US, A, 4 215 241 (PIWKNEY, Jr.). ----	

* Special categories of cited documents: [14]

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
29 January 1993	12. 02. 93
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	GRÖSSING e.h.

ANHANG

zum internationalen Recherchenbericht über die internationale Patentanmeldung Nr.

ANNEX

to the International Search Report to the International Patent Application No.

ANNEXE

au rapport de recherche international relatif á la demande de brevet international n°

PCT/GB 92/02127 SAE 67504

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Im Recherchenbericht angeführtes Patentdokument Patent document cited in search report Document de brevet cité dans le rapport de recherche	Datum der Veröffentlichung Publication date Date de publication	Mitglied(er) der Patentfamilie Patent family member(s) Membre(s) de la famille de brevets	Datum der Veröffentlichung Publication date Date de publication
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